PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Anssi Haverinen

Serial No.: 10/617,454 Art Unit: 2181

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For: DEVICE IDENTIFICATION

Attorney Docket No.: 878.0034.U1(US)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

This is an appeal from the Final Office Action dated February 28, 2006, finally rejecting claims 1-4 and 6-14 and objecting to claim 5. A Notice of Appeal and a Request for a Pre-Appeal Brief Conference were filed on May 26, 2006. A Notice of Panel Decision from Pre-Appeal Brief Review to proceed to the Board of Patent Appeals and Interferences was mailed on June 28, 2006. This Appeal Brief is herewith filed within one month of the mail date of the decision from the Pre-Appeal Brief Review. A check in the amount of $ 500 is enclosed for the filing of this appeal brief. If there are any deficiencies in payment, please charge deposit account no.: 50-1924 for any deficiency.

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TABLE OF CONTENTS

(1) REAL PARTY IN INTEREST

The real party in interest is Nokia Corporation of Espoo, Finland.

(2) RELATED APPEALS AND INTERFERENCES

The undersigned attorney is not aware of any related appeals or interferences.

(3) STATUS OF CLAIMS

The status of the claims is as follows:

Claims allowed: none

Claims objected to: 5.

Claims rejected: Claims 1-4 and 6-14.

Claims canceled: none

(4) STATUS OF AMENDMENTS AFTER FINAL

There has been one response, but no amendment proffered after the Final Office Action and a Request for Pre-Appeal Brief Review. The response after final was filed on April 11, 2006. The Patent Office mailed an advisory action on May 5, 2006. A request for a Pre-Appeal Brief Conference was filed with a Notice of Appeal on May 26, 2006. A notice of Panel Decision from Pre-Appeal Brief Review was mailed June 28, 2006, directing Applicant to proceed to the Board of Patent Appeals and Interferences.

(5) SUMMARY OF INVENTION AND CLAIMED SUBJECT MATTER

A data handling device capable of operating in a system (page 6, lines 11-12) in which two or more devices 12-14, 20 are connected by a data bus 4 for the transmission of communications therebetween, the data bus 4 having two or more data lines and the device having: two or more data bus connectors (page 8, lines 21-22), each for connection to a respective data line of the data bus 4; an identity acquisition unit 23 capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device (page 8, lines 21-23); and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus (page 8, lines 24-27) and that specify the identity stored in the data store as a destination (page 5, lines 12-16).

Claim 1 recites a data handling apparatus capable of operating in a system (page 6, lines 11-12) in which two or more devices 12-14, 20 are connected by a data bus 4 for the transmission of communications therebetween, the data bus 4 having two or more data lines and each of the two or more devices 20 having: two or more data bus connectors (page 8, lines 21-22), each for connection to a respective data line of the data bus; an identity acquisition unit 23 capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device (page 8, lines 21-23); and a data handling unit 21 capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus (page 8, lines 24-27) and that specify the identity stored in the data store as a destination (page 5, lines 12-16).

Claim 9 recites a data handling system (page 6, lines 10-12) comprising two or more data handling devices 20, each of the two or more data handling devices comprising: a data bus 4; two or more data bus connectors (page 8, lines 21-22), each for

connection to a respective data line of the data bus 4; an identity acquisition unit 23 capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device (page 8, lines 21-23); and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus (page 8, lines 24-27) and that specify the identity stored in the data store as a destination (page 5, lines 12-16).

Claim 13 recites a method for assigning an identity to each of two or more devices of a data handling apparatus capable of operating in a system in which said two or more devices 20 are connected by a data bus 4 for the transmission of communications therebetween, the data bus 4 having two or more data lines and the device 20 having two or more data bus connectors (page 8, lines 21-22, of the specification), each connected to a respective data line of the data bus 4, the method comprising: in a first mode of operation of the device, receiving data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device (page 8, lines 21-23, of the specification); and storing the identity in an identity store of the device.

ISSUES

I. Whether the Patent Office properly rejected Claims 1-4 and 6-14 under 35 U.S.C. § 103(a) as being unpatentable over Horng, U.S. Patent No. 6,738,788, in view of Dabral, U.S. Patent No. 6,192,431?

(6) ARGUMENT

ISSUE I

Did the Patent Office properly reject Claims 1-4 and 6-14 under 35 U.S.C. § 103(a) as being unpatentable over Horng, U.S. Patent No. 6,738,788, in view of Dabral, U.S. Patent No. 6,192,431?

Claims 1-14 are currently pending.

Applicant appreciates the Patent Office's indication that claim 5 has allowable subject matter, but believes that all pending claims are allowable over the prior art of record.

Claims 1, 9, and 13 to be treated separately

The Patent Office asserted (page 5, lines 10-18, of the Final Office Action mailed February 28, 2006) "As per the first argument, Horng teaches that the chip identification number are generated in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device and [see column 4, lines 34-62.] Furthermore, the examiner would like to point out that determining address/ID based on the order of the bits in one or more data word is well known in the computer art, please see pages 622-624 of the "Logic and Computer Design Fundamentals" by M. Morris Mano and Charles R. Kime. Figure 14-3 shows that the order of bits in a word determines the address."

Applicant, as discussed here and below, asserts that Horng does not teach "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..." Where in Horng is there reference to the use of the order of receipt of bits of one or more data words? The claims recite that "in response to the order in which the bits of one or more data words of a predetermined form are received" the "identity acquisition unit" determines "an identity of the device." In Horng (column 4, lines 21-24) discloses that Lofstrom, U.S. Patent No. 6161213, incorporated by reference by Horng, discloses producing a chip ID by an ID generation circuit. In Lofstrom, the

chip ID is determined through measurements, as shown in figure 8, in which the sources of paired FETs 62 are supplied from a positive power supply rail 106 in which switching of the FETs occurs through a common ROW select bit line 60 (column 7, lines 19-54, of Lofstrom). Lofstrom does not appear to disclose or fairly suggest teach "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..."

Applicant requests that the Patent Office point out with particularity where Horng discloses "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..." and other claim limitations.

Applicant has reviewed pages 622-624 of "Logic and Computer and Design Fundamentals," by M. Morris Mano and Charles R. Kime. These pages appear to disclose virtual memory and mapping main memory to cache memory, but does not appear to disclose "an identity acquisition unit ... in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device ..." or other claim limitations.

Thus, applicant believes that all pending claims are allowable over the prior art of record.

Continuing with the Patent Office's Final Office Action, pages 2-4, mailed February 28, 2006, the Patent Office has rejected claims 1-14 under 35 U.S.C. 103(a) as being unpatentable over Horng, et al., U.S. Patent No. 6,738,788, and further in view of Dabral, et al., U.S. Patent No. 6,192,431.

Claim 1 recites "A data handling apparatus capable of operating in a system in which two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and each of the two or more devices having two or more data bus connectors, each for connection to a respective data line of the data bus; **an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode**

of operation determine an identity for the device and store the identity in an identity store of the device; and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination."

Claim 9 recites "A data handling system comprising two or more data handling devices, each of the two or more data handling devices comprising a data bus; two or more data bus connectors, each for connection to a respective data line of the data bus; **an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device** and store the identity in an identity store of the device; and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination."

Claim 13 recites "A method for assigning an identity to each of two or more devices of a data handling apparatus capable of operating in a system in which said two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and the device having two or more data bus connectors, each connected to a respective data line of the data bus, the method comprising in a first mode of operation of the device, receiving data transmitted over the data bus and **in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device**; and storing the identity in an identity store of the device."

The Patent Office asserted (page 2, lines 16-21, of the Office Action mailed February 28, 2006) "an identity acquisition unit [see column 4, lines 52-62 and figure 1, element 12] capable of functioning in a first mode of operation of the device to received data transmitted over the data bus and in response to the order in which the bits or one or more data words are received on the data bus connectors during the first mode of

operation determine an identity for the device and store the identity in an identity store of the device [see column 4, lines 34-62]."

Horng recites (column 4, lines 16-62)

> The present invention relates to computer readable media storing software which, when read and executed by a conventional computer, **causes the computer to implement a database engine that keys data records to a binary number which may have randomly-positioned, non-deterministic bits. The chip ID produced by the ID generation circuit described in the aforementioned U.S. Pat. No. 6,161,213 (incorporated herein by reference) is an example of such a number.** Suitable computer-readable media for storing the software include, but are not limited to, compact disks, floppy disks, hard disks, and random access or read only memory. While the specification describes an exemplary embodiment and application of the invention considered by the applicants to be a best mode of practicing the invention, it is not intended that the invention be limited to the exemplary embodiment or to the application described below.
>
> FIG. 1 is a data flow diagram illustrating an exemplary data acquisition, storage and retrieval system 8 in accordance with the invention for storing and retrieving data relative to an IC chip (or die) 10 producing a unique ID. In the example of FIG. 1, each IC chip 10 suitably produces a 256-bit binary ID, comprising a 32-bit typeID and a 244-bit uniqueID as a key. However it should be understood that database systems in accordance with the invention may employ keys of other lengths and may be useful in contexts other than a chip identification system. The typeID field is identical for all ICs 10 of the same type, and all bits of the typeID field are deterministic, in that the ID generation circuit sets them to the same fixed values every time it generates the ID. The uniqueID field contains a number that is unique to each IC chip 10 even though a small percentage of its bits may be non-deterministic, in that the ID generation circuit may not always set them to the same value each time it generates a chip ID.
>
> System 8 includes a data acquisition system 12 such as, for example, an integrated circuit tester or any other device suitable for reading the chip ID generated by the ID generation circuit within IC chip 10. System 8 also includes a hierarchical database engine 14 in accordance with the invention for maintaining a separate "chip-type" database 16 for each possible value of the typeID field of the ID generated by IC chip 10. Database engine 14 is preferably implemented by a conventional computer programmed via software stored on computer-readable media that the conventional computer reads and executes.

Horng discloses (column 4, lines 21-24) U.S. Patent No. 6,163,213, as an example of determining a chip ID by randomly positioned, non-deterministic bits. The first paragraph in the summary of the invention of U.S. Patent No. 6,163,213, recites:

> **An integrated circuit identification (ICID) circuit** in accordance with one aspect of the invention produces a unique identification number or record (ID) for

each chip in which it is included even though the ICID circuit is fabricated on all chips using identical masks. The ICID circuit includes a set of circuit cells and **produces its output ID based on measurements of outputs of those cells that are functions of random parametric variations that naturally occur when fabricating chips.** When the number of cells is large enough, each of millions of chips can be provided with a unique identifying ID without having to customize each chip.

Apparently, Horng generates a chip identification number or code from measurements of internal chip components and not "in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device." Dabral does not remedy this deficiency of Horng since Dabral teaches a pinout may be selected (Figure 1a) by biasing a configuration I/O port to either power or ground (column 4, lines 13-26).

Thus, Horng and Dabral, alone or in combination, do not make obvious claims 1-14.

Claims 1, 9, and 13 are patentably distinct from each other as claim 1 relates to a data handling apparatus, claim 9 relates to a data handling system, and claim 13 relates to a method for assigning an identity to each of two or more devices of a data handling.

Claim 1

As claim 1 is patentably distinct from claims 9 and 13, claim 1 stands and falls alone.

Claim 9

As claim 9 is patentably distinct from claims 1 and 13, claim 9 stands and falls alone.

Claim 13

As claim 13 is patentably distinct from claims 1 and 9, claim 13 stands and falls alone.

Claim 2

Claim 2 recites "wherein the identity acquisition unit is arranged to process each of the one or more data words of a predetermined form in accordance with a look-up table in order to determine the identity for the device." As to claim 2, Horng (column 4, lines 34-62) does not appear to disclose or fairly suggest a lookup table. A hierarchical

database engine is not a lookup table. Thus, claim 2 is allowable over the prior art of record for this additional reason.

The Patent Office asserted (last four lines of the Final Office Action mailed February 28, 2006) "As per the second argument, Horng teaches wherein the identity acquisition unit is arranged to process the or each data word of a predetermined form in accordance with a look-up table in order to determine the identity for the device [see Horng column 4, lines 34-62, 'database' and column 3, lines 42-49, 'database system'.]

Applicant submits that a database is not a lookup table nor is a database system a lookup table. From http://en.wikipedia.org/wiki/Associative_array , "An **associative array** (also known as a map, lookup table, or dictionary and in query-processing as an index or index file) is an abstract data type composed of a collection of keys and a collection of values, where each key is associated with one value. The operation of finding the value associated with a key is called a *lookup* or indexing, and this is the most important operation supported by an associative array. The relationship between a key and its value is sometimes called a mapping or binding. For example, if the value associated with the key `"bob"` is `7`, we say that our array *maps* `"bob"` to `7`. Associative arrays are very closely related to the mathematical concept of a function with a finite domain..."

According to Wikipedia's definition of a database, http://72.14.203.104/search?q=cache:LORcdd1Nj6cJ:en.wikipedia.org/wiki/Database+wikipedia+database&hl=en&gl=us&ct=clnk&cd=1 , "A database is an organized collection of data. The term originated within the computer industry, but its meaning has been broadened by popular use, to the extent that the European Database Directive (which creates intellectual property rights for databases) includes non-electronic databases within its definition. This article is confined to a more technical use of the term; though even amongst computing professionals, some attach a much wider meaning to the word than others."

Horng does not disclose or fairly suggest a lookup table. The term "key," as referred to by Horng (column 4, lines 34-62) is formed of a typeID and the generated unique ID. Thus, claim 2 is allowable over the prior art of record.

Claim 3

Claim 3 recites "A data handling apparatus as claimed in claim 1, comprising a multiplexing arrangement located between the data bus connectors and the data handling unit and arranged to, in at least the second mode of operation, re-order in accordance with the stored identity data received from at least two of the data lines of the bus and passed to the data handling unit." Although Horng discloses "storing and retrieving data relative to an IC chip (or die) 10 producing a unique ID and each IC chip 10 suitably produces a binary ID (col. 4, lines 35-40), Horng appears to rely on U.S. Patent No. 6,161,213 (col. 4, line 22) to Lofstrom which teaches that chip ID generation is accomplished through the performance of each chip where each chip determines its own address. Horng does not appear to disclose a need for using a multiplexing arrangement that is arranged to re-order in accordance with stored identity data received from at least two of the data lines of the bus... Even arguing a combination of Horng and Dabral would not lead to the claimed invention because Dabral's multiplexer is concerned with providing a pinout that is used to reduce signal path length (col. 4, lines 58-63) and avoid cross routing (col. 4, lines 40-43) and not "re-order in accordance with the stored identity data." Thus, claim 3 is allowable over the prior art of record.

Claim 3 is patentably distinct from claims 1, 2, 9, and 13 and stands and falls alone.

Claim 4

Claim 4 recites "A data handling apparatus as claimed in claim 3, wherein the multiplexing arrangement is a hardware multiplexing arrangement." As discussed above, Horng has no need or desire for a multiplexing arrangement. Dabral discloses a multiplexer that changes the pinout of an integrated circuit. Neither Horng nor Dabral, alone or in combination, disclose or fairly suggest a hardware multiplexing arrangement that re-orders in accordance with the stored identity data received from at least two of the data lines of the bus and passed to the data handling unit. Thus, claim 4 is allowable over the prior art of record.

Claim 4 is patentably distinct from claims 1-3, 9, and 13 and stands and falls alone.

Claim 6

Claim 6 recites "A data handling apparatus as claimed in claim 1, wherein the device is a data processor." As the Patent Office did not treat claim 6 on the merits in the Final Office Action dated February 28, 2006, it is presumed that claim 6 has allowable subject matter. Horng does not appear to disclose the IC chip 10 is a data processor. Dabral does not appear to remedy this deficiency. Thus, claim 6 is allowable over the prior art of record.

Claim 6 is patentably distinct from claims 1-4, 9, and 13 and stands and falls alone.

Claim 7

Claim 7 recites "A data handling apparatus as claimed in claim 1, wherein the device is a memory device." Contrary to the assertion by the Patent Office in the Final Office Action dated February 28, 2006, (page 4, lines 1-3), Horng does not appear to identify the IC chips for which a database is described are memory devices. Thus, claim 7 is allowable over the prior art of record.

Claim 7 is patentably distinct from claims 1-4, 6, 9, and 13 and stands and falls alone.

Claim 8

Claim 8 recites "A data handling apparatus as claimed in claim 1, wherein the device is defined on an integrated circuit and the data bus connectors are connectors for communicating to and/or from the integrated circuit." Neither Horng nor Dabral appear to disclose or fairly suggest a device defined on an integrated circuit (claim 8) in which the device has an identity acquisition unit and a data handling unit (from claim 1, included in claim 8). Thus, claim 8 is allowable over the prior art of record.

Claim 8 is patentably distinct from claims 1-4, 6, 7, 9, and 13 and stands and falls alone.

Claim 10

Claim 10 recites "A data handling system as claimed in claim 9, comprising a further device connected to the bus and capable of functioning to transmit the said one or more data words of a predetermined form over the data bus." Horng discloses that the IC 10 transmits a unique ID to a database which then uses this unique ID to select the

appropriate database for storing data relative to that IC (col. 4, lines 63-65). Dabral is concerned with rearranging pin out and, like Horng, is not concerned with transmitting one or more data words of a predetermined form over the data bus. Thus, claim 10 is allowable over the prior art.

Claim 10 is patentably distinct from claims 1-4, 6-9, and 13 and stands and falls alone.

Claim 11

Claim 11 recites "A data handling system as claimed in claim 10, wherein the further device is capable of triggering the data handling devices to enter the first mode of operation." Horng (col. 4, lines 34-62; col. 1, lines 14-37) appears to be silent regarding the subject matter "wherein the further device is capable of triggering the data handling devices to enter the first mode of operation" of claim 11. Dabral does not appear to remedy this deficiency. Thus, claim 11 is allowable over the prior art of record.

Claim 11 is patentably distinct from claims 1-4, 6-10, and 13 and stands and falls alone.

Claim 12

Claim 12 recites "A data handling system as claimed in claim 10, wherein the data handling devices are arranged to automatically enter the first mode of operation upon initialisation of the system." Horng (col. 4, lines 34-62; col. 1, lines 14-37) appears to be silent regarding the subject matter "wherein the data handling devices are arranged to automatically enter the first mode of operation upon initialisation of the system" of claim 12. Dabral does not appear to remedy this deficiency. Thus, claim 12 is allowable over the prior art of record.

Claim 12 is patentably distinct from claims 1-4, 6-11, and 13 and stands and falls alone.

Claim 14

Claim 14 recites "A method as claimed in claim 13, comprising: in a second mode of operation of the device, handling by means of a data handling unit of the device communications transmitted over the bus and that specify the identity stored in the data store as a destination." Horng does not appear to disclose IC 10 has a second mode of operation for "handling by means of a data handling unit of the device communications

transmitted over the bus and that specify the identity stored in the data store as a destination." Dabral does not appear to remedy this deficiency. Thus, claim 14 is allowable over the prior art of record.

Claim 14 is patentably distinct from claims 1-4 and 6-13 and stands and falls alone.

The Patent Office in the advisory action mailed May 5, 2006, stated (Box 11) "The request for reconsideration has been considered but does not place the application in condition for allowance because Horng teaches the chip identification number are generated in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device and (see column 4, lines 34-62). Furthermore, the examiner would like to point out that determining address/ID based on the order of the bits in one or more data word is well know in the computer art, please see pages 622-264 of the "Logic and Computer Design Fundamentals" by M. Morris Mano and Charles R. Kime. Figure 14-3 shows that the order of bits in a word determines the address. Horng teaches wherein the identity acquisition unit is arranged to process the or each data word of a predetermined form in accordance with a look-up table in order to determine the identity for the device (see Horng column 4, lines 34-62, 'database' and column 3, lines 42-49, 'database system').

Horng, as discussed above, does not disclose or fairly suggest the claimed subject matter of "in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device." Neither Dabral nor Mano, as has been discussed, remedy this deficiency. Mano, in Figure 14-3, uses a portion of the main memory address as the cache memory address and does not appear to disclose or fairly suggest the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors ... determine an identity for the device.

It is respectfully submitted that all claims 1-14 are allowable over the prior art of record.

Applicant thanks the Patent Office for the indication of allowable subject matter in claim 5.

The Patent Office is respectfully requested to reconsider and remove the rejections of the claims 1-4 and 6-14 under 35 U.S.C. 103(a) based on Horng and Dabral, and to allow all of the pending claims 1-14 as now presented for examination. An early notification of the allowability of claims 1-14 is earnestly solicited.

CONCLUSION

For the above reasons, it is respectfully requested that in each of the rejections discussed herein under 35 U.S.C. § 103(a), the Patent Office has failed to meet the burden in establishing a prima facie basis for the rejections of Claims 1-14. Accordingly, reversal of all outstanding rejections is earnestly solicited.

Respectfully submitted,

Dated: July 28, 2006

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7-28-06 Ann Okrentowicz

Date

(8) CLAIMS APPENDIX

1. A data handling apparatus capable of operating in a system in which two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and each of the two or more devices having:

two or more data bus connectors, each for connection to a respective data line of the data bus;

an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device; and

a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination.

2. A data handling apparatus as claimed in claim 1, wherein the identity acquisition unit is arranged to process each of the one or more data words of a predetermined form in accordance with a look-up table in order to determine the identity for the device.

3. A data handling apparatus as claimed in claim 1, comprising a multiplexing arrangement located between the data bus connectors and the data handling unit and arranged to, in at least the second mode of operation, re-order in accordance with the stored identity data received from at least two of the data lines of the bus and passed to the data handling unit.

4. A data handling apparatus as claimed in claim 3, wherein the multiplexing arrangement is a hardware multiplexing arrangement.

5. A data handling apparatus as claimed in claim 3, wherein the identity acquisition unit is arranged to determine the identity in accordance with a deviation in the order of at least some of the bits of each of the one or more data words from a standard order, and the multiplexing arrangement is arranged to re-order the data lines of the bus so as to restore the standard order to the bits as applied to the data handling unit.

6. A data handling apparatus as claimed in claim 1, wherein the device is a data processor.

7. A data handling apparatus as claimed in claim 1, wherein the device is a memory device.

8. A data handling apparatus as claimed in claim 1, wherein the device is defined on an integrated circuit and the data bus connectors are connectors for communicating to and/or from the integrated circuit.

9. A data handling system comprising two or more data handling devices, each of the two or more data handling devices comprising:

a data bus;

two or more data bus connectors, each for connection to a respective data line of the data bus;

an identity acquisition unit capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device; and

a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination.

10. A data handling system as claimed in claim 9, comprising a further device connected to the bus and capable of functioning to transmit the said one or more data words of a predetermined form over the data bus.

11. A data handling system as claimed in claim 10, wherein the further device is capable of triggering the data handling devices to enter the first mode of operation.

12. A data handling system as claimed in claim 10, wherein the data handling devices are arranged to automatically enter the first mode of operation upon initialisation of the system.

13. A method for assigning an identity to each of two or more devices of a data handling apparatus capable of operating in a system in which said two or more devices are connected by a data bus for the transmission of communications therebetween, the data bus having two or more data lines and the device having two or more data bus connectors, each connected to a respective data line of the data bus, the method comprising:

in a first mode of operation of the device, receiving data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identity for the device; and

storing the identity in an identity store of the device.

14. A method as claimed in claim 13, comprising:

in a second mode of operation of the device, handling by means of a data handling unit of the device communications transmitted over the bus and that specify the identity stored in the data store as a destination.

(9) EVIDENCE APPENDIX

Applicant proffers no evidence.

(10) RELATED PROCEEDINGS APPENDIX

The undersigned attorney is not aware of any related appeals or interferences.